

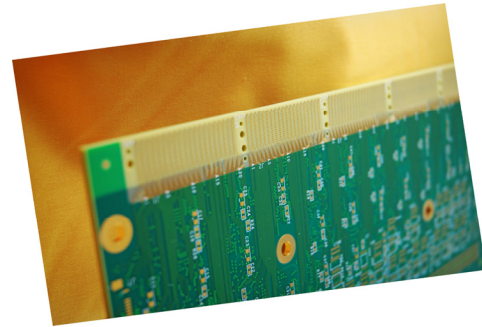
rigid line card

Whether it's simple-sided, thru-hole work to bleeding-edge HDI applications, we can provide your organization with the technology you need. Many designs today are constructed with lower layer counts and less real estate. This pushes our suppliers to produce finer lines & smaller vias within a confined space. All of the rigid boards that we supply are electronically tested and certified under UL standards. Please review our capabilities below.

Standard Features	Standard	Advanced
Inner-layer Trace / Space (0.5 oz)	.004/.004	.002/.002
Outer-layer Trace / Space (1 oz)	.005/.005	.002/.002
Pad Over Drill Size for Tangency (drill + x)	.010	.008
Antipad (Clearance) Over Drill Size	.020	.016
Minimum Mechanical Drill Size	.010	.006
Minimum Core Thickness	.002	.001
Maximum Copper Weight	3 oz	7 oz
Minimum Copper Weight	.5 oz	.125 oz
Maximum Aspect Ratio	10:1	22:1
Maximum Layer Count	30+	30+
Maximum Board Thickness	≤ .125	.250
Minimum Board Thickness	.021	.008
Solder Mask Registration	± .002	± .0015

Micro-Via Features	Standard	Advanced
Minimum μ -Via Hole Size	.004	.004
Maximum Aspect Ratio	.7:1	1:1
Capture/Target Pad Over Drill Size	.008	.004
μ -Via Hole Plug	Y	Y
Glass Reinforced Dielectrics [UV/CO2 Dual Laser]	Y	Y
Stacked Vias	N	Y

Materials	Standard	Advanced
FR-4 (min 170Tg (DSC)) Standard	Y	Y
Polymide	Y	Y
Getek/Megtron (PPO)	Y	Y
Isola (all except 640 Series and IS500)	Y	Y
Isola IS640	N	Y
BC2000	Y	Y
Rogers 4000 Series	Y	Y
Rogers 3000, 5000, 6000, TMM Series	N	Y
Arlon	N	Y
Nelco 4000, 5000, 7000, 8000, 9000 Series	N	Y
Thermagon	Y	Y
Gore Speedboard C, Speedboard N	N	Y
Bromine Free	N	Y
Taconics	N	Y



Surface Finishes	Standard	Advanced
HASL	Y	Y
ENIG	Y	Y
Electrolytic Ni/Au	Y	Y
Immersion Sn	Y	Y
Immersion Ag	Y	Y
Selective Finishes	N	Y
Wire Bondable Soft Electrolytic AU	Y	Y
SnPb Reflow	N	Y
OSP	Y	Y

Other	Standard	Advanced
Buried Core Vias	Y	Y
Sequential Lamination	Y	Y
Optical Drill	Y	Y
Impedance (Single Ended & Differential)	±10%	±5%
Buried Capacitance (Planar/Discrete)	Y	Y
Buried Resistors	N	Y
Chip Cavity	N	Y
Mixed Dielectrics	Y	Y
Conductive / Non-Conductive Hole Fill	Y	Y
Metal Core (Al, Cu)	N	Y
Depth Control Drill / Rout	Y	Y
Etchback (Plasma)	Y	Y

**1: .002/.002 [50/50] achievable assuming improvements in LDI resolution (6000+ DPI)

**2: Assuming CAF resistant laminate

**3: Minimum drill-size is dependent on aspect ratio.

**4: Dependent on design

Specifications as of May 17, 2010
Specifications are subject to change without notice.